Instruction Manual

Tektronix

TMS444
SH7750 Microprocessor Software Support

071-1048-00

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Preface

This instruction manual contains specific information about the TMS444 SH7750 microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS444 SH7750 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor support packages is included with each product. Each logic analyzer includes basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the target system
- Setting up the logic analyzer to acquire data from the target system
- Acquiring and viewing disassembled data

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that identifies bus cycles and displays cycle types.
- The phrase “information on basic operations” refers to logic analyzer online help, or a user manual covering the basic operations of the microprocessor support.
- The term “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.

Contacting Tektronix

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*** This phone number is toll free in North America. After office hours, please leave a voice mail message.**
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

Getting Started

Getting Started

This section contains information on the TMS444 SH7750 microprocessor support and information on connecting your logic analyzer to your target system.

Support Package Description

The TMS444 microprocessor support package provides state only support and software that decodes and displays the cycle types for systems based on the Hitachi SH7750 microprocessors. This support does not decode the instructions.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS444 SH7750 microprocessor support.

To use this support efficiently, you need the items listed in the information on basic operations as well as the

- Hitachi SuperH RISC engine SH7750 Series (SH7750, SH7750S) Hardware Manual ADE-602-124C Rev. 4.0 4/21/00 Hitachi, Ltd.
- SH7750 High Performance RISC Engine Programming Manual ADE-602-156A Rev. 2.0 03/04/99 Hitachi, Ltd.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software this support is compatible with.

Logic Analyzer Configuration

The TMS444 SH7750 support requires a minimum of one 136-channel 100 MHz acquisition module.

Requirements and Restrictions

Review electrical specifications in the *Specifications* section in this manual as they pertain to your target system, as well as the following descriptions of other TMS444 SH7750 support requirements and restrictions.

Hardware Reset. If a hardware reset occurs in your TMS444 SH7750 system during an acquisition, the application disassembler might acquire invalid samples.

System Clock Rate. The TMS444 SH7750 microprocessor support can acquire data from the SH7750 microprocessor operating at speeds of up to 100 MHz[1]. If the bus speed is 100MHz, then for proper acquisition the support requires the use of 200 MHz acquisition module. The TMS444 SH7750 microprocessor support has been tested for bus speeds of 66 MHz.

Channel Groups. Channel groups required for clocking and disassembly are:

- Address
- Data_Hi
- Data_Lo
- Control
- ChipSelect
- WE_CAS
- Mode
- SDRAM
- SRAM
- BROM (burstable ROM)
- PCMCIA

In the Misc group, no signals (except CKIO signal) are required for clocking and disassembly.

Nonintrusive Acquisition. Acquiring microprocessor bus cycles is nonintrusive to the target system. That is, the TMS444 SH7750 does not intercept, modify or present back signals to the target system.

Disabling the Instruction Cache. To display disassembled acquired data, you must disable the internal instruction cache. Disabling the cache makes all instruction prefetches visible on the bus so that they can be acquired and their corresponding cycle types are displayed.

1 Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.

Disabling the Data Cache. To display acquired data, you must disable the data cache. Disabling the data cache makes visible on the bus all of the loads and stores to memory, including data reads and writes, so that the software can acquire and display them.

Timing Display Format

A Timing Display Format file is provided for the support. It sets up the display to show the following waveforms:

- Address
- Data_Hi
- Data_Lo
- Control
- BS~
- RDY~
- RD/WR~
- ChipSelect
- WE_CAS

NOTE. *Address, Data_Hi, Data_Lo, Control, ChipSelect and WE_CAS are displayed in busform.*

The method of selecting or restoring the Timing Display Format file is different for each platform and is ignored in this document.

Functionality Not Supported

Alternate Bus Master. Alternate bus master transactions are not processed in the disassembly.

Memory Types. The following memory types are simply identified. Their cycles are not analyzed.

- MPX
- DRAM

- Byte Control SRAM (BCSRAM)

Functionality Not Tested

The following functionalities are supported but not tested.

- PCMCIA Cycles
- SRAM Write Cycles
- BROM Cycles
- Little Endian Mode

Connecting the Logic Analyzer to a Target System

You can use the channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make the connections between the logic analyzer and your target system.

To connect the probes to SH7750 signals in the target system using a test clip, follow the steps:

1. Power off your target system. It is not necessary to power off the logic analyzer.

CAUTION. *To prevent static damage, handle the microprocessor, probes, and the logic analyzer module in a static-free environment. Static discharge can damage these components.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored electricity from the test clip.

CAUTION. *To prevent permanent damage to the pins on the microprocessor, place the target system on a horizontal surface before connecting the test clip.*

3. Place the target system on a horizontal, static-free surface.
4. Use Tables 3–4 through 3–17 starting on page 3–3 to connect the channel probes to SH7750 signal pins on the test clip or in the target system.

5. Use leadsets to connect at least one ground lead from each channel and the ground lead from each clock probe to the ground pins on your test clip.

Operating Basics

Setting Up the Support

This section provides information on how to set up the support and covers the following topics:

- Clocking options
- Timing diagram

The information in this section is specific to the operations and functions of the TMS444 SH7750 support on any Tektronix logic analyzer for which the support can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and display disassembled data, you need to load the support and specify the setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Installing the Support Software

***NOTE**. Before you install any software, it is recommended you verify that the microprocessor support software is compatible with the logic analyzer software.*

To install the TMS444 SH7750 software on your Tektronix logic analyzer, follow these steps:

1. Insert the floppy disk in the disk drive.
2. Click the Windows Start button, point to Settings, and click Control Panel.
3. In the Control Panel window, double-click Add/Remove Programs.
4. Follow the instructions on the screen for installing the software from the floppy disk.

To remove or uninstall software, follow the above instructions and select Uninstall. You need to close all windows before you uninstall any software.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the TMS444 SH7750 support are Address, Data_Hi, Data_Lo, Control, ChipSelect, WE_CAS, Misc, Mode, SDRAM, SRAM, BROM and PCMCIA. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–2.

Clocking

Acquisition Setup

The SH7750 affects the logic analyzer setup menus (and submenus) by modifying existing fields and adding microprocessor-specific fields.

On the logic analyzer, the SH7750 adds the selection “SH7750” to the Load Support Package dialog box, under the File pulldown menu. Once that “SH7750” has been loaded, the “Custom” clocking mode selection in the logic analyzer module Setup menu is also enabled.

Clocking Options

The TMS444 SH7750 support offers a microprocessor-specific clocking mode for the SH7750 microprocessor. This clocking mode is the default selection whenever you load the TMS444 SH7750 support.

Disassembly is not correct when using the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

Custom Clocking

A special clocking program is loaded to the module every time you load the TMS444 SH7750 support. This special clocking is called Custom.

In this support, with Custom Clocking, the module logs in signals from multiple channel groups at every rising edge of the CKIO signal. The module then sends all the logged in signals to the trigger machine and to the acquisition memory of the module for storage.

In Custom clocking, the module clocking state machine (CSM) generates one master sample for each rising edge of the clock signal CKIO.

When Custom is selected, the Custom Clocking Options menu displays the subtitle “SH7750 Clocking”, and displays the Clocking Option Sample On — Rising Edge of CKIO. This is the default and the only option available.

Bus Timing Diagram. CKIO is the clockout signal. At every rising edge of CKIO, all the signals are sampled and mastered for all memory types. A basic timing for SDRAM Burst Read is given in Figure 2–1.

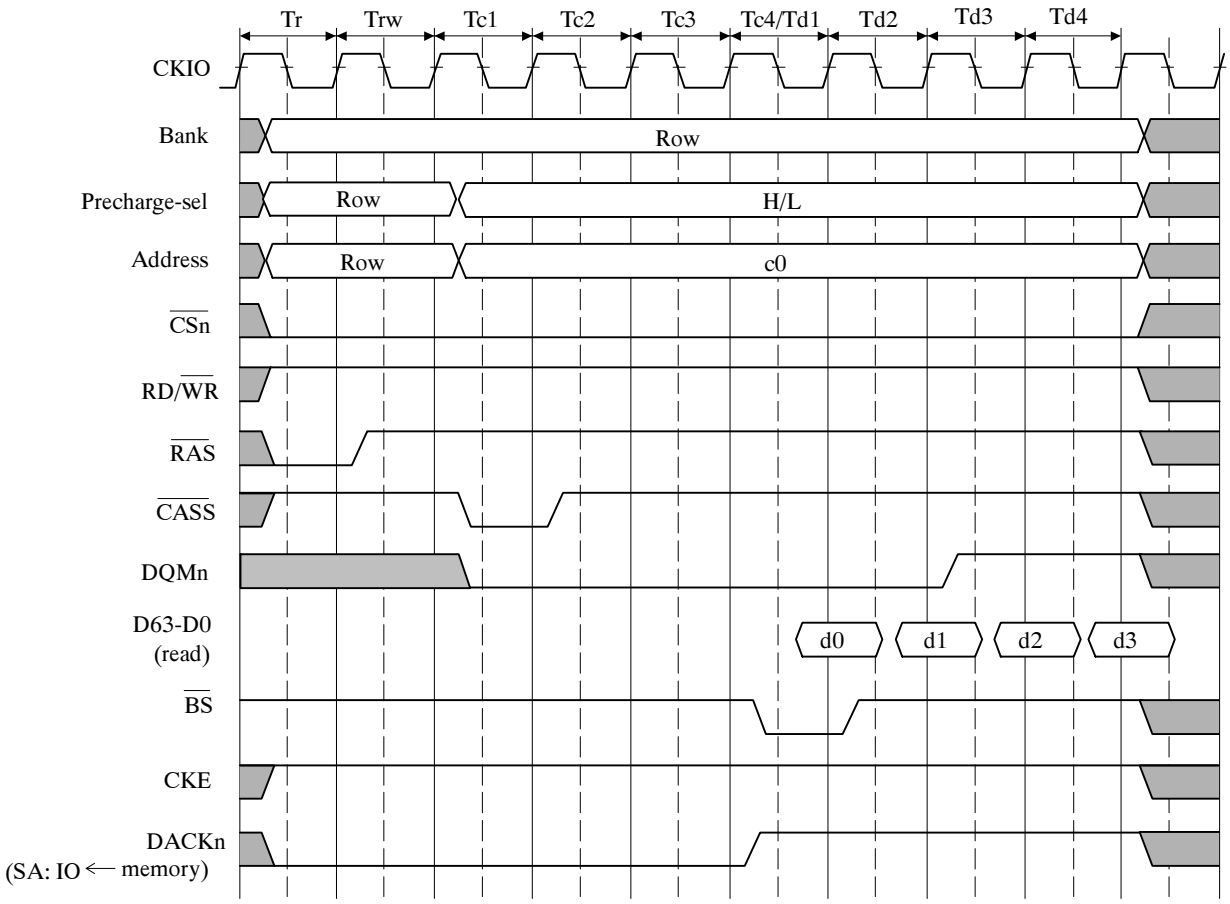


Figure 2-1: Basic timing for SDRAM Burst Read

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics and tasks:

- Acquiring data
- Viewing disassembled data in various display formats
- Viewing cycle type labels
- Changing the way data is displayed

Acquiring Data

Once you load the TMS444 SH7750 support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your logic analyzer online help or *Appendix A: Error Messages and Disassembly Problems* in the user manual.

Viewing Disassembled Data

You can view disassembled data in the following display formats:

All (This the default display format)
No Idles/Waits

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2-11.*

The default display format shows the Address, Data_Hi, Data_Lo, Control, ChipSelect and WE_CAS channel group values for each sample of acquired data.

If a channel group is not visible, you must use the Add Column (Ctrl+L) to make the group visible.

Timing Display Format

The timing-waveform display format file is provided for the logic analyzer 700 Series support. The timing-waveform display format file sets up and displays the following waveforms:

This is the standard logic analyzer Waveform display. It sets up the display to show the following waveforms:

Address	(busform)
Data_Hi	(busform)
Data_Lo	(busform)
Control	(busform)
BS~	
RDY~	
RD/WR~	
ChipSelect	(busform)
WE_CAS	(busform)

With the logic analyzer, this file must be loaded before an acquisition is taken.

"All" Display Format

In the "All" display format, the disassembler displays cycle type labels in parentheses. The following tables list the cycle type labels and give the definitions of the cycle they represent for all the supported memory types.

Table 2–1 lists these cycle type labels for BROM (Burstable ROM) and definitions of the cycles they represent.

Table 2-1: BROM cycle type label definitions

Cycle type	Definition
(BROM - T1 Read Start)	Bus Read Start
(BROM - T1 Write Start)	Bus Write Start
(BROM - Read Data)	Data Read
(BROM - Write Data)	Data Write
(BROM - TB1 Cycle)	TB1 Cycle
(BROM - TS1 Cycle)	TS1 (Setup) State
(BROM - TH1 Cycle)	TH1 (Hold) State
(BROM - TH2 Cycle)	TH2 (Hold) State
(BROM - TH3 Cycle)	TH3 (Hold) State
(BROM - WAIT Cycle)	Wait State
(BROM Cycle)	BROM Cycle

Table 2–2 lists the cycle type labels for SDRAM and definitions of the cycles they represent.

Table 2-2: SDRAM cycle type label definitions

Cycle type	Definition
(SDRAM - Tpr Cycle)	Pre-Charge
(SDRAM - Tpc Cycle)	Pre-Charge
(SDRAM - Trw Cycle)	Row Address Wait
(SDRAM - Tr Cycle)	Row Address Start
(SDRAM - Tc1 Cycle)	Tc1 Cycle
(SDRAM - Tc2 Cycle)	Tc2 Cycle
(SDRAM - Tc3 Cycle)	Tc3 Cycle
(SDRAM - Tc4 Cycle)	Tc4 Cycle
(SDRAM(RAS DOWN) - Tr Cycle)	Tr Cycle (RAS Down Mode)
(SDRAM - TMw1 Cycle)	SDRAM TMw1 Cycle
(SDRAM(RAS DOWN) - TRp1 Cycle)	TRp1 Cycle (RAS Down Mode)
(SDRAM Refresh)	Refresh Cycle
(SDRAM(RAS DOWN) - D1 Write Data)	Write Data (RAS Down Mode)
(SDRAM - Tc1 Single Write Data)	Single Write Data
(SDRAM - Tc1 D1 Write Data)	Write Data
(SDRAM - Tc2 D2 Write Data)	Write Data
(SDRAM - Tc3 D3 Write Data)	Write Data
(SDRAM - Tc4 D4 Write Data)	Write Data
(SDRAM - Td1 D1 Read Data)	Read Data
(SDRAM - Td2 D2 Read Data)	Read Data
(SDRAM - Td3 D3 Read Data)	Read Data
(SDRAM - Td4 D4 Read Data)	Read Data
(SDRAM Cycle)	SDRAM Cycle

Table 2–3 lists these cycle type labels for SRAM and definitions of the cycles they represent.

Table 2-3: SRAM cycle type label definitions

Cycle type	Definition
(SRAM - T1 Read Start)	Bus Read Start
(SRAM - T2 Read Data)	Data Read
(SRAM - T1 Write Start)	Bus Write Start
(SRAM - T2 Write Data)	Data Write
(SRAM - WAIT Cycle)	Wait Cycle
(SRAM Cycle)	SRAM Cycle

Table 2–4 lists the cycle type labels for PCMCIA and definitions of the cycles they represent.

Table 2-4: PCMCIA cycle type label definitions

Cycle type	Definition
(PCMCIA - Memory Read Start)	Bus Read Start
(PCMCIA - Memory Read Data)	Data Read
(PCMCIA - Memory Write Start)	Bus Write Start
(PCMCIA - Memory Write Data)	Data Write
(PCMCIA - I/O Read Start)	Bus Read Start
(PCMCIA - I/O Read Data)	Data Read
(PCMCIA - I/O Write Start)	Bus Write Start
(PCMCIA - I/O Write Data)	Data Write
(PCMCIA - WAIT Cycle)	Wait Cycle
(PCMCIA - Hold Wait)	Hold Wait
(PCMCIA Cycle)	PCMCIA Cycle

Table 2–5 lists the cycle type labels for MPX and definitions of the cycles they represent.

Table 2-5: MPX cycle type label definitions

Cycle type	Definition
(MPX - Cycle)	Any MPX Cycle

Table 2–6 lists the cycle type labels for DRAM and definitions of the cycles they represent.

Table 2-6: DRAM cycle type label definitions

Cycle type	Definition
(DRAM - Cycle)	Any DRAM Cycle

Table 2–7 lists the cycle type labels for BCSRAM (Byte Control SRAM) and definitions of the cycles they represent.

Table 2-7: BCSRAM cycle type label definitions

Cycle type	Definition
(BCSRAM - Cycle)	Any BCSRAM Cycle

Table 2–8 lists the General cycle type labels and the definitions of the cycles they represent.

Table 2-8: General cycle type label definitions

Cycle types	Definition
(RESET)	Reset
(MANUAL RESET)	Manual Reset
(Idle Cycle)	Idle Cycle
(No devices selected)	No devices selected
(UNKNOWN)	Unknown combination

Figure 2–2 displays an example of the “All” display format.

Sample	SH7750 Address	SH7750 Data_Hi	SH7750 Data_Lo	SH7750 Mnemonics	SH7750 Control	SH7750 ChipSelect	SH7750 WE_CAS	Timestamp
653	0C001010	--------	--------	(SDRAM - Tc2 Cycle)	READ	CS3-	11110000	15.000 ns
654	0C001010	--------	6D436E63	(SDRAM - Td1 D1 Read Data)	BUS START	CS3-	11110000	15.000 ns
655	0C001018	--------	6D136F13	(SDRAM - Td2 D2 Read Data)	READ	CS3-	11110000	15.000 ns
656	0C001020	--------	65436763	(SDRAM - Td3 D3 Read Data)	READ	CS3-	11110000	15.000 ns
657	0C001028	--------	61C361E3	(SDRAM - Td4 D4 Read Data)	READ	CS3-	11111111	15.000 ns
659	0C001000	--------	--------	(SDRAM - Tr Cycle)	READ	CS3-	11111111	30.000 ns
660	0C001008	--------	--------	(SDRAM - Trw Cycle)	READ	CS3-	00001111	15.000 ns
661	0C001000	--------	--------	(SDRAM - Tc1 Cycle)	READ	CS3-	00001111	15.000 ns
662	0C001018	--------	--------	(SDRAM - Tc2 Cycle)	READ	CS3-	00001111	15.000 ns
663	0C001018	6F836B13	--------	(SDRAM - Td1 D1 Read Data)	BUS START	CS3-	00001111	15.000 ns
664	0C001020	61036323	--------	(SDRAM - Td2 D2 Read Data)	READ	CS3-	00001111	15.000 ns
665	0C001028	698361A3	--------	(SDRAM - Td3 D3 Read Data)	READ	CS3-	00001111	15.000 ns
666	0C001030	6B036C23	--------	(SDRAM - Td4 D4 Read Data)	READ	CS3-	11111111	15.000 ns
668	0C001000	--------	--------	(SDRAM - Tr Cycle)	READ	CS3-	11111111	30.000 ns
669	0C001008	--------	--------	(SDRAM - Trw Cycle)	READ	CS3-	11110000	15.000 ns
670	0C001000	--------	--------	(SDRAM - Tc1 Cycle)	READ	CS3-	11110000	15.000 ns
671	0C001018	--------	--------	(SDRAM - Tc2 Cycle)	READ	CS3-	11110000	15.000 ns
672	0C001018	--------	6D136F13	(SDRAM - Td1 D1 Read Data)	BUS START	CS3-	11110000	14.500 ns
673	0C001020	--------	65436763	(SDRAM - Td2 D2 Read Data)	READ	CS3-	11110000	15.500 ns
674	0C001028	--------	61C361E3	(SDRAM - Td3 D3 Read Data)	READ	CS3-	11110000	15.000 ns
675	0C001030	--------	6D436E63	(SDRAM - Td4 D4 Read Data)	READ	CS3-	11111111	15.000 ns
677	0C001000	--------	--------	(SDRAM - Tr Cycle)	READ	CS3-	11111111	30.000 ns
678	0C001008	--------	--------	(SDRAM - Trw Cycle)	READ	CS3-	00001111	15.000 ns
679	0C001000	--------	--------	(SDRAM - Tc1 Cycle)	READ	CS3-	00001111	15.000 ns
680	0C001020	--------	--------	(SDRAM - Tc2 Cycle)	READ	CS3-	00001111	15.000 ns
681	0C001020	6A036923	--------	(SDRAM - Td1 D1 Read Data)	BUS START	CS3-	00001111	15.000 ns
682	0C001028	6A833BAC	--------	(SDRAM - Td2 D2 Read Data)	READ	CS3-	00001111	15.500 ns
683	0C001030	68036623	--------	(SDRAM - Td3 D3 Read Data)	READ	CS3-	00001111	15.000 ns
684	0C001038	63833BAC	--------	(SDRAM - Td4 D4 Read Data)	READ	CS3-	11111111	15.000 ns
686	0C001000	--------	--------	(SDRAM - Tr Cycle)	READ	CS3-	11111111	29.500 ns
687	0C001008	--------	--------	(SDRAM - Trw Cycle)	READ	CS3-	11110000	15.000 ns
688	0C001000	--------	--------	(SDRAM - Tc1 Cycle)	READ	CS3-	11110000	15.000 ns
689	0C001020	--------	--------	(SDRAM - Tc2 Cycle)	READ	CS3-	11110000	15.000 ns
690	0C001020	--------	67436463	(SDRAM - Td1 D1 Read Data)	BUS START	CS3-	11110000	15.000 ns
691	0C001028	--------	33CC35EC	(SDRAM - Td2 D2 Read Data)	READ	CS3-	11110000	15.000 ns
692	0C001030	--------	63436D63	(SDRAM - Td3 D3 Read Data)	READ	CS3-	11110000	15.500 ns
693	0C001038	--------	3DCC3FEC	(SDRAM - Td4 D4 Read Data)	READ	CS3-	11111111	14.500 ns
695	0C001000	--------	--------	(SDRAM - Tr Cycle)	READ	CS3-	11111111	30.000 ns
696	0C001008	--------	--------	(SDRAM - Trw Cycle)	READ	CS3-	00001111	15.000 ns
697	0C001000	--------	--------	(SDRAM - Tc1 Cycle)	READ	CS3-	00001111	15.000 ns
698	0C001028	--------	--------	(SDRAM - Tc2 Cycle)	READ	CS3-	00001111	15.000 ns
699	0C001028	6A833BAC	--------	(SDRAM - Td1 D1 Read Data)	BUS START	CS3-	00001111	15.000 ns
700	0C001030	68036623	--------	(SDRAM - Td2 D2 Read Data)	READ	CS3-	00001111	15.000 ns

Figure 2-2: Example of the “All “ display format

“No Idles/Waits” Display Format

In “No Idles/Waits” display format only the data cycles are displayed. Other bus cycles such as Bus starts, Waits and Idles are suppressed. The data cycles type labels given in Tables 2–1 through 2–8 are displayed in this format.

Table 2–9 lists the cycle type label definitions and definitions of the cycles they represent.

Table 2-9: Cycle type label definitions in “No Idles/Waits” display format

Cycle type	Definition
(BROM - Read Data)	Data Read
(BROM - Write Data)	Data Write
(SDRAM - Tc1 Single Write Data)	Single Write Data
(SDRAM - Tc1 D1 Write Data)	Write Data

Table 2- 9: Cycle type label definitions in "No Idles/Waits" display format (Cont.)

Cycle type	Definition
(SDRAM(RAS DOWN) - D1 Write Data)	Write Data
(SDRAM - Tc2 D2 Write Data)	Write Data
(SDRAM - Tc3 D3 Write Data)	Write Data
(SDRAM - Tc4 D4 Write Data)	Write Data
(SDRAM - Td1 D1 Read Data)	Read Data
(SDRAM - Td2 D2 Read Data)	Read Data
(SDRAM - Td3 D3 Read Data)	Read Data
(SDRAM - Td4 D4 Read Data)	Read Data
(SRAM - T2 Read Data)	Read Data
(SRAM - T2 Write Data)	Write Data
(PCMCIA - Memory Read Data)	Read Data
(PCMCIA - Memory Write Data)	Write Data
(PCMCIA - I/O Read Data)	Read Data
(PCMCIA - I/O Write Data)	Write Data
(MPX - Cycle)	Any MPX Cycle
(DRAM - Cycle)	Any DRAM Cycle
(BCSRAM - Cycle)	Any BCSRAM Cycle

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the TMS444 SH7750 support to do the following tasks:

- Change how data is displayed across all display formats
- Display exception cycles

Optional Display Selections

You can make optional selections for disassembled data. Refer to the information on basic operations for more information.

Displaying Exception Labels

The disassembler can display SH7750 exception labels. The exception table must reside in external memory for interrupt and exception cycles to be visible to the disassembler.

Enter the Vector Base Address in the Vector Base Register field. This field is located in the Disassembly property page (Disassembly Format Definition overlay).

Table 2–10 lists the SH7750 interrupt and exception labels.

Table 2-10: Interrupt and exception labels

Offset	Displayed interrupt or exception name
0x00100	(GENERAL EXCEPTION)
0x00400	(INTERRUPT-COMPLETION TYPE)
0x00600	(TLB DATA/INST MISS EXCEPTION)

Disassembly Display Options

Table 2-11: Logic analyzer disassembly display options

Description	Option	
Show:	All No Idles/Waits	(Default)
Highlight:	No Idles/Waits None	(Default)
Disassemble Across Gaps:	Yes No	 (Default)

Micro Specific Fields

After you load the TMS444 SH7750 support, choose a clocking mode and specify the trigger. Open the Disassembly window by right clicking on the Listing window and selecting Properties. The following paragraph lists the options:

Memory type connected to each of the seven areas. Choose the memory connected to each area using the drop-down bar. If no device is connected to a particular area, select “No Device”. By default the selection is “No Device”.

AREA 0 (CS0~): Choose the memory type connected to AREA 0 by selecting one of the options.

Area 0 (CS0~):	No Device	(default)
	SRAM	
	BROM	
	MPX	

AREA 1 (CS1~): Choose the memory type connected to AREA 1 by selecting one of the options.

Area 1 (CS1~):	No Device	(default)
	SRAM	
	BCSRAM	
	MPX	

AREA 2 (CS2~): Choose the memory type connected to AREA 2 by selecting one of the options.

Area 2 (CS2~):	No Device	(default)
	SRAM	
	SDRAM	
	DRAM	
	MPX	

AREA 3 (CS3~): Choose the memory type connected to AREA 3 by selecting one of the options.

Area 3 (CS3~):	No Device	(default)
	SRAM	
	SDRAM	
	DRAM	
	MPX	

AREA 4 (CS4~): Choose the memory type connected to AREA 4 by selecting one of the options.

Area 4 (CS4~):	No Device	(default)
	SRAM	
	BCSRAM	
	MPX	

AREA 5 (CS5~): Choose the memory type connected to AREA 5 by selecting one of the options.

Area 5 (CS5~):	No Device	(default)
	SRAM	
	BROM	
	PCMCIA	
	MPX	

AREA 6 (CS6~): Choose the memory type connected to AREA 6 by selecting one of the options.

Area 6 (CS6~):	No Device	(default)
	SRAM	
	BROM	
	PCMCIA	
	MPX	

***NOTE**. If nonburstable Flash Memory is used, select the SRAM option.*

AREA0 SRAM Bus Width. Choose the Bus Width of the SRAM connected.

AREA0 SRAM Bus Width:	32	(default)
	64	
	16	
	8	

AREA1 SRAM Bus Width. Choose the Bus Width of the SRAM connected.

AREA1 SRAM Bus Width:	32	(default)
	64	
	16	
	8	

AREA2 SRAM Bus Width. Choose the Bus Width of the SRAM connected.

AREA2 SRAM Bus Width:	32	(default)
	64	
	16	
	8	

AREA3 SRAM Bus Width. Choose the Bus Width of the SRAM connected.

AREA3 SRAM Bus Width:	32	(default)
	64	
	16	
	8	

AREA4 SRAM Bus Width. Choose the Bus Width of the SRAM connected.

AREA4 SRAM Bus Width:	32	(default)
	64	
	16	
	8	

AREA5 SRAM Bus Width. Choose the Bus Width of the SRAM connected.

AREA5 SRAM Bus Width:	32	(default)
	64	
	16	
	8	

AREA6 SRAM Bus Width. Choose the Bus Width of the SRAM connected.

AREA6 SRAM Bus Width:	32	(default)
	64	
	16	
	8	

BROM Bus Width. Choose the width of the bus connected to the BROM by selecting one of the options.

BROM Bus Width:	32 bits	(default)
	16 bits	
	8 bits	

SDRAM Bus Width. Choose the width of the bus connected to the SDRAM by selecting one of the options.

SDRAM Bus Width:	32 bits	(default)
	64 bits	

PCMCIA- AREA 5 Bus. Choose the width of the bus connected to the PCMCIA in AREA 5 by selecting one of the options.

PCMCIA–AREA 5:	Fixed	(default)
	Dynamic	

PCMCIA- AREA 6 Bus. Choose the width of the bus connected to the PCMCIA in AREA 6 by selecting one of the options.

PCMCIA–AREA 6:	Fixed	(default)
	Dynamic	

PCMCIA- AREA 5 Hold. Choose the number of PCMCIA Hold Wait states.

PCMCIA–AREA 5 Hold:	15	(default)
	12	
	9	
	6	
	3	
	2	
	1	
	0	

PCMCIA- AREA 6 Hold. Choose the number of PCMCIA Hold Wait states.

PCMCIA–AREA 6 Hold:	15	(default)
	12	
	9	
	6	
	3	
	2	
	1	
	0	

AREA 0 WAIT STATES. Choose the number of wait states for the device connected to this area.

AREA 0 WAIT STATES:	15	(default)
	12	
	9	
	6	
	3	
	2	
	1	
	0	

AREA 1 WAIT STATES. Choose the number of wait states for the device connected to this area.

AREA 1 WAIT STATES:	15	(default)
	12	
	9	
	6	
	3	
	2	
	1	
	0	

AREA 2 WAIT STATES. Choose the number of wait states for the device connected to this area.

AREA 2 WAIT STATES:	15	(default)
	12	
	9	
	6	
	3	
	2	
	1	
	0	

AREA 3 WAIT STATES. Choose the number of wait states for the device connected to this area.

AREA 3 WAIT STATES:	15	(default)
	12	
	9	
	6	
	3	
	2	
	1	
	0	

AREA 4 WAIT STATES. Choose the number of wait states for the device connected to this area.

AREA 4 WAIT STATES:	15	(default)
	12	
	9	
	6	
	3	
	2	
	1	
	0	

AREA 5 WAIT STATES. Choose the number of wait states for the device connected to this area.

AREA 5 WAIT STATES:	15	(default)
	12	
	9	
	6	
	3	
	2	
	1	
	0	

AREA 6 WAIT STATES. Choose the number of wait states for the device connected to this area.

AREA 6 WAIT STATES:	15	(default)
	12	
	9	
	6	
	3	
	2	
	1	
	0	

AREA 0 WAIT BY RDY~. Choose the wait state insertion by RDY~ pin by selecting one of the options.

AREA 0 WAIT BY RDY~:	ZERO	(default)
	NON-ZERO	

AREA 1 WAIT BY RDY~. Choose the wait state insertion by RDY~ pin by selecting one of the options.

AREA 1 WAIT BY RDY~:	ZERO	(default)
	NON-ZERO	

AREA 2 WAIT BY RDY~. Choose the wait state insertion by RDY~ pin by selecting one of the options.

AREA 2 WAIT BY RDY~:	ZERO	(default)
	NON-ZERO	

AREA 3 WAIT BY RDY~. Choose the wait state insertion by RDY~ pin by selecting one of the options.

AREA 3 WAIT BY RDY~:	ZERO	(default)
	NON-ZERO	

AREA 4 WAIT BY RDY~. Choose the wait state insertion by RDY~ pin by selecting one of the options.

AREA 4 WAIT BY RDY~:	ZERO	(default)
	NON-ZERO	

AREA 5 WAIT BY RDY~. Choose the wait state insertion by RDY~ pin by selecting one of the options.

AREA 5 WAIT BY RDY~:	ZERO	(default)
	NON-ZERO	

AREA 6 WAIT BY RDY~. Choose the wait state insertion by RDY~ pin by selecting one of the options.

AREA 6 WAIT BY RDY~:	ZERO	(default)
	NON-ZERO	

AMX Setting. The AMX setting is required for the Address Multiplexing feature of SDRAM. For example, for a bus width of 32 bits, when four banks of (1Meg*8bit*2) are connected the AMX selection is 1.

AMX Setting:	0	(default)
	1	
	2	
	3	
	4	
	5	
	6	
	7	

AMXEXT Setting. The AMXEXT setting is required for the Address Multiplexing feature of SDRAM. For example, for a bus width of 32 bits, when four banks of (1Meg*8bit*2) are connected the AMXEXT selection is 0.

AMXEXT Setting:	0	(default)
	1	

BROM Setup. Choose the number of BROM setup cycles introduced.

BROM Setup:	0	(default)
	1	

BROM Hold. Choose the number of BROM hold cycles introduced.

BROM Hold:	0	(default)
	1	
	2	
	3	

Vector Base Register. Enter the contents of the 32 bit Vector Base Register. The default value is 0x00000000.

After choosing the options, you are ready to acquire and disassemble data. If you have any problems acquiring data, refer to information on basic operations in your online help or in the user manual.

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided on your software disk to view an example of how your SH7750 microprocessor bus cycles looks when they are disassembled. Viewing this system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your target system.

Information on basic operations describes how to view the file.

Reference

Reference:Tables

This section lists the symbol tables and channel assignment tables for disassembly and timing.

Symbol Tables

The TMS444 SH7750 support supplies two symbol-table files. The SH7750_Ctrl file replaces specific Control-channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 3–1 shows the definitions for name, bit pattern and meaning of the Control group symbols in file SH7750_Ctrl.

Table 3-1: SH7750_Ctrl group symbol table definitions

Symbol	Control group value RESET~ MRESET~ BS~ RDY~ RAS~ RD/CASS~ RD/WR~	Description
RESET	0 X X X X X X	Reset
MANUAL RESET	X 0 X X X X X	Manual reset
WRITE	1 1 0 X X X 0	Write
BUS START	1 1 0 X X X X	Bus start
READ	1 1 X X X X 1	Read
WRITE	1 1 X X X X 0	Write

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as for the Address channel group.

Table 3–2 shows the definitions for name, bit pattern, and meaning of the ChipSelect group symbols.

Table 3-2: SH7750_ChipSelect group symbol table definitions

Symbol	ChipSelect group value												Description
	MD3CE2A~	MD4CE2B~				CS6~			CS5~			CS4~	CS3~				CS2~			CS1~			CS0~	
NO DEVICE	X	X	1	1	1	1	1	1	1	1			No device
CS0~	X	X	1	1	1	1	1	1	1	0			CS0~
CS1~	X	X	1	1	1	1	1	0	1				CS1~
CS2~	X	X	1	1	1	1	0	1	1				CS2~
CS3~	X	X	1	1	1	0	1	1	1				CS3~
CS4~	X	X	1	1	0	1	1	1	1				CS4~
CS5~	X	X	1	0	1	1	1	1	1				CS5~
CS5~	0	1	1	1	1	1	1	1	1				CS5~
CS6~	X	X	0	1	1	1	1	1	1				CS6~
CS6~	1	0	1	1	1	1	1	1	1				CS6~
MORE DEVICES	X	X	X	X	X	X	X	X	X				MORE DEVICES

Channel Assignment Tables

Channel assignments shown in Table 3–3 through Table 3–17 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal.

Table 3–3 displays the order in which the channel group assignments are displayed.

Table 3-3: Channel assignment groups

Group name	Display radix
Address	Hexadecimal
Data_Hi	Hexadecimal

Table 3-3: Channel assignment groups (Cont.)

Group name	Display radix
Data_Lo	Hexadecimal
Control	Symbolic
ChipSelect	Symbolic
WE_CAS	BIN
Misc	OFF
Mode	OFF
SDRAM	OFF
SRAM	OFF
BROM	OFF
PCMCIA	OFF

Table 3–4 shows the channel assignments for the logic analyzer Address group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-4: Address group channel assignments

Bit order	Section:channel	SH7750 support channel name
25	A3:1	A25
24	A3:0	A24
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	AA
11	A1:3	A11
10	A1:2	A10

Table 3-4: Address group channel assignments (Cont.)

Bit order	Section:channel	SH7750 support channel name
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1
0	A0:0	A0

Table 3–5 shows the probe section and channel assignments for the Data_Hi group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-5: Data_Hi group channel assignments

Bit order	Section:channel	SH7750 support channel name
31	E3:7	D63
30	E3:6	D62
29	E3:5	D61
28	E3:4	D60
27	E3:3	D59
26	E3:2	D58
25	E3:1	D57
24	E3:0	D56
23	E2:7	D55
22	E2:6	D54
21	E2:5	D53
20	E2:4	D52
19	E2:3	D51
18	E2:2	D50
17	E2:1	D49
16	E2:0	D48

Table 3-5: Data_Hi group channel assignments (Cont.)

Bit order	Section:channel	SH7750 support channel name
15	E1:7	D47
14	E1:6	D46
13	E1:5	D45
12	E1:4	D44
11	E1:3	D43
10	E1:2	D42
9	E1:1	D41
8	E1:0	D40
7	E0:7	D39
6	E0:6	D38
5	E0:5	D37
4	E0:4	D36
3	E0:3	D35
2	E0:2	D34
1	E0:1	D33
0	E0:0	D32

Table 3–6 shows the probe section and channel assignments for the Data_Lo group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-6: Data_Lo group channel assignments

Bit order	Section:channel	SH7750 support channel name
31	D3:7	D31
30	D3:6	D30
29	D3:5	D29
28	D3:4	D28
27	D3:3	D27
26	D3;2	D26
25	D3:1	D25
24	D3:0	D24
23	D2:7	D23
22	D2:6	D22

Table 3-6: Data_Lo group channel assignments (Cont.)

Bit order	Section:channel	SH7750 support channel name
21	D2:5	D21
20	D2:4	D20
19	D2:3	D19
18	D2:2	D18
17	D2:1	D17
16	D2:0	D16
15	D1:7	D15
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8
7	D0:7	D7
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3
2	D0:2	D2
1	D0:1	D1
0	D0:0	D0

Table 3–7 shows the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. By default, this channel group is displayed as symbols. The symbol table file name is SH7750_Ctrl.

Table 3-7: Control group channel assignments

Bit order	Section:channel	SH7750 support channel name
6	Q0	RESET~
5	C2:0	MRESET~
4	Clock:2	BS~

Table 3-7: Control group channel assignments (Cont.)

Bit order	Section:channel	SH7750 support channel name
3	Clock:3	RDY~
2	Clock:1	RAS~
1	C2:2	RD/CASS~
0	C2:1	RD/WR~

Table 3–8 shows the probe section and channel assignments for the ChipSelect group and the microprocessor signal to which each channel connects. By default, this channel group is displayed as binary.

Table 3-8: ChipSelect group channel assignments

Bit order	Section:channel	SH7750 support channel name
8	C2:6	MD3CE2A~
7	C2:7	MD4CE2B~
6	C1:6	CS6~
5	C1:5	CS5~
4	C1:4	CS4~
3	C1:3	CS3~
2	C1:2	CS2~
1	C1:1	CS1~
0	C1:0	CS0~

Table 3–9 shows the probe section and channel assignments for the logic analyzer WE_CAS group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3-9: WE_CAS group channel assignments

Bit order	Section:channel	SH7750 support channel name
7	C0:7	WE/CAS7~
6	C0:6	WE/CAS6~
5	C0:5	WE/CAS5~
4	C0:4	WE/CAS4~
3	C0:3	WE/CAS3~
2	C0:2	WE/CAS2~

Table 3-9: WE_CAS group channel assignments (Cont.)

Bit order	Section:channel	SH7750 support channel name
1	C0:1	WE/CAS1~
0	C0:0	WE/CAS0~

Table 3–10 shows the probe section and channel assignments for the logic analyzer Misc group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3-10: Misc group channel assignments

Bit order	Section:channel	SH7750 support channel name
7	Clock:0	CKIO
6	Qual:3	DACK1
5	Qual:2	DACK0
4	A3:3	DREQ1~
3	A3:2	DREQ0~
2	A3:5	DRAK1
1	A3:4	DRAK0
0	C1:7	NMI

Table 3–11 shows the probe section and channel assignments for the logic analyzer Mode group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3-11: Mode group channel assignments

Bit order	Section:channel	SH7750 support channel name
8	C3:3	MD8~
7	C3:2	MD7~
6	C3:1	MD6~
5	C3:0	MD5~
4	C2:7	MD4CE2B~
3	C2:6	MD3CE2A~
2	C2:5	MD2~
1	C2:4	MD1~
0	C2:3	MD0~

Table 3–12 shows the probe section and channel assignments for the logic analyzer SDRAM group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3-12: SDRAM group channel assignments

Bit order	Section:channel	SH7750 support channel name
3	Clock:1	RAS~
2	C2:2	RD/CASS~
1	Clock:2	BS~
0	C2:1	RD/WR~

Table 3–13 shows the probe section and channel assignments for the logic analyzer SRAM group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3-13: SRAM group channel assignments

Bit order	Section:channel	SH7750 support channel name
3	Clock:2	BS~
2	C2:1	RD/WR~
1	C2:2	RD/CASS~
0	Clock:3	RDY~

Table 3–14 shows the probe section and channel assignments for the logic analyzer BROM group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3-14: BROM group channel assignments

Bit order	Section:channel	SH7750 support channel name
3	Clock:2	BS~
2	Clock:3	RDY~
1	C2:1	RD/WR~
0	C2:2	RD/CASS~

Table 3–15 shows the probe section and channel assignments for the logic analyzer PCMCIA group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3-15: PCMCIA group channel assignments

Bit order	Section:channel	SH7750 support channel name
10	Clock:2	BS~
9	Clock:3	RDY~
8	C2:1	RD/WR~
7	C2:2	RD/CASS~
6	C0:1	WE/CAS1~
5	C0:2	WE/CAS2~
4	C0:3	WE/CAS3~
3	C0:7	WE/CAS7~
2	C2:6	MD3CE2A~
1	C2:7	MD4CE2B~
0	C3:1	MD6

Table 3–16 shows the probe section and channel assignments for the clock probes (not part of any group) and the SH7750 signal to which each channel connects.

Table 3-16: Clock channel assignments

Logic analyzer section & probe	SH7750 support package channel name	AMP Mictor pin number
Clock:3	RDY~	C5
Clock:2	BS~	D6
Clock:1	RAS~	A6
Clock:0	CKIO	A5

Table 3–17 shows the probe section and qualifier channel assignments.

Table 3-17: Qualifier channel assignments

Logic analyzer section & probe	SH7750 support package channel name	AMP Mictor pin number
QUAL:3	DACK1	E5
QUAL:2	DACK0	E6
QUAL:1	------	--
QUAL:0	RESET~	D5

Since the acquisition is Clock by Clock, Clock:2-0, C2:3-0 and QUAL:3-0, are used as Data, not as qualifiers.

CPU To Mictor Connections

For design purposes, you may need to make connections between the CPU and the Mictor pins of the P6434 Mass Termination Probe. Refer to the *P6434 Mass Termination Probe* manual, Tektronix part number 070-9793-XX, for more information on mechanical specifications. Tables 3–19 through 3–22 show the CPU pin to Mictor pin connections.

***NOTE**. To preserve signal quality in the target system, it is recommended that a 180 Ω resistor is connected in series between each ball pad of the CPU and each pin of the Mictor connector. The resistor must be within 1/2 inch of the ball pad of the CPU.*

The recommended pin assignment is the AMP pin assignment, because the AMP circuit board layout model and other commercial CAD packages use the Amp numbering scheme. See Table 3–18.

Table 3-18: Recommended pin assignments for a Mictor connector (component side)

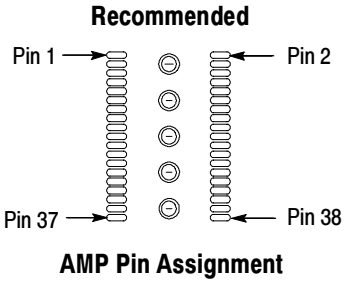
Graphic column	Text column
	Recommended. This pin assignment is the industry standard and is what we recommend that you use.

Table 3-19: CPU to Mictor connections for AMP Mictor A pins

Logic analyzer channel	AMP Mictor A pin number	SH7750 support channel name	QFP208 Package pin number
NC	1	-	-
NC	2	-	-
NC	3	-	-
NC	4	-	-
CLOCK1	6	RAS~	93

Table 3-19: CPU to Mictor connections for AMP Mictor A pins (Cont.)

Logic analyzer channel	AMP Mictor A pin number	SH7750 support channel name	QFP208 Package pin number
CLOCK0	5	CKIO	77
A3:7	7	BREQ/BSACK~	52
A3:6	9	-	-
A3:5	11	DRAK1	85
A3:4	13	DRAK0	86
A3:3	15	DREQ1~	107
A3:2	17	DREQ0~	106
A3:1	19	A25	180
A3:0	21	A24	179
A2:7	23	A23	176
A2:6	25	A22	175
A2:5	27	A21	174
A2:4	29	A20	173
A2:3	31	A19	172
A2:2	33	A18	171
A2:1	35	A17	62
A2:0	37	A16	63
A1:7	8	A15	64
A1:6	10	A14	67
A1:5	12	A13	68
A1:4	14	A12	71
A1:3	16	A11	72
A1:2	18	A10	73
A1:1	20	A9	74
A1:0	22	A8	75
A0:7	24	A7	76
A0:6	26	A6	80
A0:5	28	A5	81
A0:4	30	A4	82
A0:3	32	A3	83
A0:2	34	A2	84

Table 3-19: CPU to Mictor connections for AMP Mictor A pins (Cont.)

Logic analyzer channel	AMP Mictor A pin number	SH7750 support channel name	QFP208 Package pin number
A0:1	36	A1	189
A0:0	38	A0	186

Table 3-20: CPU to Mictor connections for AMP Mictor C pins

Logic analyzer channel	AMP Mictor C pin number	SH7750 support channel name	QFP208 Package pin number
NC	1	-	-
NC	2	-	-
NC	3	-	-
NC	4	-	-
CLOCK3	5	RDY~	1
QUAL1	6	-	-
C3:7	7	BACK/BSREQ~	51
C3:6	9	CKE	55
C3:5	11	STATUS1	191
C3:4	13	STATUS0	190
C3:3	15	MD8/RTS2~	166
C3:2	17	MD7/TXD	167
C3:1	19	MD6/IOIS16~	92
C3:0	21	MD5/RAS2~	183
C2:7	23	MD4/CE2B~	182
C2:6	25	MD3/CE2A~	181
C2:5	27	MD2/RXD2	151
C2:4	29	MD1/TXD2	150
C2:3	31	MD0/SCK	149
C2:2	33	RD~/CASS~/FRAME~	94
C2:1	35	RD/WR~	95
C2:0	37	SCK2/MRESET~	168
C1:7	8	NMI	156
C1:6	10	CS6~	7

Table 3-20: CPU to Mictor connections for AMP Mictor C pins (Cont.)

Logic analyzer channel	AMP Mictor C pin number	SH7750 support channel name	QFP208 Package pin number
C1:5	12	CS5~	6
C1:4	14	CS4~	5
C1:3	16	CS3~	89
C1:2	18	CS2~	90
C1:1	20	CS1~	4
C1:0	22	CS0~	3
C0:7	24	WE7~/CAS7~/DQM7/REG~	101
C0:6	26	WE6~/CAS6~/DQM6	98
C0:5	28	WE5~/CAS5~/DQM5~	58
C0:4	30	WE4~/CAS4~/DQM4~	59
C0:3	32	WE3~/CAS3~/DQM3~/ICIOWR~	97
C0:2	34	WE2~/CAS2~/DQM2~/ICIORD~	96
C0:1	36	WE1~/CAS1~/DQM1	60
C0:0	38	WE0~/CAS0~/DQM0	61

Table 3-21: CPU to Mictor connections for AMP Mictor D pins

Logic analyzer channel	AMP Mictor D pin number	SH7750 support channel name	QFP208 Package pin number
NC	1	-	-
NC	2	-	-
NC	3	-	-
NC	4	-	-
CLOCK2	6	BS~	8
QUAL0	5	RESET~	2
D3:7	7	D31	124
D3:6	9	D30	122
D3:5	11	D29	120
D3:4	13	D28	116
D3:3	15	D27	112
D3:2	17	D26	110

Table 3-21: CPU to Mictor connections for AMP Mictor D pins (Cont.)

Logic analyzer channel	AMP Mictor D pin number	SH7750 support channel name	QFP208 Package pin number
D3:1	19	D25	108
D3:0	21	D24	103
D2:7	23	D23	102
D2:6	25	D22	104
D2:5	27	D21	109
D2:4	29	D20	111
D2:3	31	D19	115
D2:2	33	D18	119
D2:1	35	D17	121
D2:0	37	D16	123
D1:7	8	D15	33
D1:6	10	D14	35
D1:5	12	D13	37
D1:4	14	D12	41
D1:3	16	D11	45
D1:2	18	D10	47
D1:1	20	D9	49
D1:0	22	D8	53
D0:7	24	D7	54
D0:6	26	D6	50
D0:5	28	D5	48
D0:4	30	D4	46
D0:3	32	D3	42
D0:2	34	D2	38
D0:1	36	D1	36
D0:0	38	D0	34

Table 3-22: CPU to Mictor connections for AMP Mictor E pins

Logic analyzer channel	AMP Mictor E pin number	SH7750 support channel name	QFP208 Package pin number
NC	1	-	-
NC	2	-	-
NC	3	-	-
NC	4	-	-
QUAL3	5	DACK1	185
QUAL2	6	DACK0	184
E3:7	7	D63	146
E3:6	9	D62	142
E3:5	11	D61	140
E3:4	13	D60	138
E3:3	15	D59	134
E3:2	17	D58	132
E3:1	19	D57	130
E3:0	21	D56	128
E2:7	23	D55	127
E2:6	25	D54	129
E2:5	27	D53	131
E2:4	29	D52	133
E2:3	31	D51	137
E2:2	33	D50	139
E2:1	35	D49	141
E2:0	37	D48	145
E1:7	8	D47	11
E1:6	10	D46	15
E1:5	12	D45	17
E1:4	14	D44	19
E1:3	16	D43	23
E1:2	18	D42	25
E1:1	20	D41	27
E1:0	22	D40	29
E0:7	24	D39	30

Table 3-22: CPU to Mictor connections for AMP Mictor E pins (Cont.)

Logic analyzer channel	AMP Mictor E pin number	SH7750 support channel name	QFP208 Package pin number
E0:6	26	D38	28
E0:5	28	D37	26
E0:4	30	D36	24
E0:3	32	D35	20
E0:2	34	D34	18
E0:1	36	D33	16
E0:0	38	D32	12

Channel Assignments with AMP Mictor Connector diagrams for SH7750 QFP208 Package

The Figures 3–1 through 3–4 show the channel assignments with the AMP Mictors for the SH7750 QFP208 package.

Channel Assignment Diagram for AMP Mictor A

SH7750 Signal	QFP208 PIN Number	AMP MICTOR			QFP208 PIN Number	SH7750 Signal
		1		2		
		3	GND	4		
CKIO	77	5		6	93	RAS~
BREQ~/BSACK~	52	7		8	64	A15
		9		10	67	A14
DRAK1	85	11	GND	12	68	A13
DRAK0	86	13		14	71	A12
DREQ1~	107	15		16	72	A11
DREQ0~	106	17		18	73	A10
A25	180	19	GND	20	74	A9
A24	179	21		22	75	A8
A23	176	23		24	76	A7
A22	175	25		26	80	A6
A21	174	27	GND	28	81	A5
A20	173	29		30	82	A4
A19	172	31		32	83	A3
A18	171	33		34	84	A2
A17	62	35	GND	36	189	A1
A16	63	37		38	186	A0

Figure 3- 1: Channel assignments for AMP Mictor A

Channel Assignment Diagram for AMP Mictor C

SH7750 Signal	QFP208 PIN Number	AMP MICTOR			QFP208 PIN Number	SH7750 Signal
		1		2		
		3	GND	4		
RDY~	1	5		6		
BACK~/BSREQ~	51	7		8	156	NMI
CKE	55	9		10	7	CS6~
STATUS1	191	11	GND	12	6	CS5~
STATUS0	190	13		14	5	CS4~
MD8/RTS2~	166	15		16	89	CS3~
MD7/TXD	167	17		18	90	CS2~
MD6/IOIS16~	192	19	GND	20	4	CS1~
MD5/RAS2~	183	21		22	3	CS0~
MD4/CE2B~	182	23		24	101	WE7~/CAS7~/DQM7/REG~
MD3/CE2A~	181	25		26	98	WE6~/CAS6~/DQM6
MD2/RXD2	151	27	GND	28	58	WE5~/CAS5~/DQM5
MD1/TXD2	150	29		30	59	WE4~/CAS4~/DQM4
MD0/SCK	149	31		32	97	WE3~/CAS3~/DQM3/ICIOWR~
RD~/CASS~/FRAME~	94	33		34	96	WE2~/CAS2~/DQM2/ICIORD~
RD/WR~	95	35	GND	36	60	WE1~/CAS1~/DQM1
SCK2/MRESET~	168	37		38	61	WE0~/CAS0~/DQM0

Figure 3- 2: Channel assignments for AMP Mictor C

Channel Assignment Diagram for AMP Mictor D

SH7750 Signal	QFP208 PIN Number	AMP MICTOR			QFP208 PIN Number	SH7750 Signal
		1		2		
		3	GND	4		
RESET~	2	5		6	8	BS~
D31	124	7		8	33	D15
D30	122	9		10	35	D14
D29	120	11	GND	12	37	D13
D28	116	13		14	41	D12
D27	112	15		16	45	D11
D26	110	17		18	47	D10
D25	108	19	GND	20	49	D9
D24	103	21		22	53	D8
D23	102	23		24	54	D7
D22	104	25		26	50	D6
D21	109	27	GND	28	48	D5
D20	111	29		30	46	D4
D19	115	31		32	42	D3
D18	119	33		34	38	D2
D17	121	35	GND	36	36	D1
D16	123	37		38	34	D0

Figure 3-3: Channel assignments for AMP Mictor D

Channel Assignment Diagram for AMP Mictor E

SH7750 Signal	QFP208 PIN Number	AMP MICTOR			QFP208 PIN Number	SH7750 Signal
		1		2		
		3	GND	4		
DACK1	185	5		6	184	DACK0
D63	146	7		8	11	D47
D62	142	9		10	15	D46
D61	140	11	GND	12	17	D45
D60	138	13		14	19	D44
D59	134	15		16	23	D43
D58	132	17		18	25	D42
D57	130	19	GND	20	27	D41
D56	128	21		22	29	D40
D55	127	23		24	30	D39
D54	129	25		26	28	D38
D53	131	27	GND	28	26	D37
D52	133	29		30	24	D36
D51	137	31		32	20	D35
D50	139	33		34	18	D34
D49	141	35	GND	36	16	D33
D48	145	37		38	12	D32

Figure 3- 4: Channel assignments for AMP Mictor E

Specifications

Specifications

This section contains information regarding the specifications of the support.

Specification Tables

Table 4–1 lists the electrical requirements the target system must produce for the support to acquire correct data.

Table 4-1: Electrical specifications

Characteristics	Requirements
Target system clock rate	
SH7750 specified clock rate	Max 100 MHz
SH7750 tested clock rate	Max 66 MHz
Minimum setup time required	
Logic analyzer	2.5 ns
Minimum hold time required	
Logic analyzer	0 ns

Replaceable Parts List

Replaceable Parts List

This section contains a list of the replaceable components and modules for the TMS444 SH7750 support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Using the Replaceable Parts List

The tabular information in the Replaceable Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
80009	TEKTRONIX, INC.	P.O. BOX 500	BEAVERTON, OR, 97077-0001

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					STANDARD ACCESSORIES		
	071-1048-00			1	MANUAL,TECH INSTRUCTIONS,SH7750;TMS444	80009	071-1048-00

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